(Figure 1). Hence, the trench profile, via CD and height, and chamfer angle will vary in trenches depending on their width. Hard mask selectivity also becomes a concern for the dense trenches where the hard mask at smaller dimensions is more significantly affected by sputtering. Recently, the concept of atomic layer etching and quasi-atomic layer etch (Q-ALE) has been widely used in various applications for high selectivity requirements and ideal bottom trench profile engineering[1,2]. However, little studying has been done on sub 40nm pitch BEOL dielectric etch with Q-ALE.

In this work, we investigate the impacts of Q-ALE on low-K materials compared to continuous wave (CW) plasma and pulsed plasma. We demonstrate that Q-ALE can be successfully used to suppress RIE lag in BEOL low-K materials at advanced pitches. In order to minimize low-K damage generated during the etching process, an inverse RIE lag process was also developed. These processes can be used with conventional etching processes to compensate RIE lag and result in optimum process performance (Figure 2). In addition, Q-ALE technique shows improved hard mask selectivity and results in lower pattern roughness. Finally, combining Q-ALE and CW processes can minimize wafer throughput impact from Q-ALE processes, which usually take significantly longer than CW processes (Figure 3).

References:

[1] S. D. Sherpa and A. Ranjan, J. Vac. Sci. Technol. A, **35**, 01A102, (2017)

[2] M. Wang, P. L. G. Ventzek, and A. Ranjan, J. Vac. Sci. Technol. A, **35**, 03130, (2017)

Keywords: RIE lag, quasi-ALE, pulsed plasma, low-K damage

2:00pm **ALE1-TuA3 Precise Etching Profile Control by Atomic-scale Process*, Yoshihide Kihara,*** *T. Katsunuma, M. Tabata, T. Hisamatsu, M. Honda,* Tokyo Electron Miyagi Ltd., Japan **INVITED**

In recent years, with the progress of device miniaturization and increased challenges in the scale of integration as semiconductor devices, fine control of the surface reactions is required in the fabrication processes. In self-aligned contacts (SAC) process, ultra-high selectivity of SiO_2 etching towards SiN is required, for which we developed Quasi-ALE technique for SiO_2 etching. Quasi-ALE precisely controls the reaction layer thickness of the surface, by controlling the radical and ion flux independently. In Quasi-ALE, adsorption step contains radical supply onto the surface and activation step contains etching by ion bombardment. Quasi-ALE was able to improve the conventional trade-off between the etching ability on the micro slit portions and SiN selectivity in the SAC process [1].

We have advanced Quasi-ALE technology for control of etching profile. The advanced technology is called as rapid advanced cyclic etching (RACE) process. The RACE process is divided by process gas into several steps that have a different purpose as a function of each process gas. As a result, we can easily set optimum radical and ion fluxes and ion energy for each step. Therefore, RACE process enables even more precise control of the surface reactions.

TiN mask pattern is transferred to the underlying SiO_2 and low-k film in metal hard mask trench process of BEOL where TiN mask selectivity, chamfer profile control and critical dimension (CD) variation at wafer very edge are the big patterning challenges. In the conventional method, the process results show that there is a trade-off between TiN mask selectivity and chamfer profile. To address this issue, RACE process was adopted in BEOL trench process. With this method, we were able to control the chamfer profile while keeping a low TiN mask loss. This is because RACE process achieves very fine control of the surface reactions by maximizing the effect of each step in RACE process. In addition, RACE process was able to reduce the CD variation at wafer very edge. This is demonstrating that RACE process is effective technique for not only the etching performance but also the CD uniformity.

On the other hand, we developed new CD shrinking technique without CD loading that combines Atomic Layer Deposition (ALD) and etching [2]. To control etching profile precisely, ALD was adopted to various applications. In the presentation, we will introduce some etching performances.

1. M. Honda, T. Katsunuma, M. Tabata, A. Tsuji, T. Oishi, T. Hisamatsu, S. Ogawa and Y. Kihara, J. Phys. D: Appl. Phys. 50, 234002 (2017)

2. M. Honda, “New Innovative Dielectric Etching Approaches by Controlling the Surface Reaction at Atomic-Level” 4th ALE 2017

Atomic Layer Etching
Room 104-106 - Session ALE2-TuA

Selective ALE

Moderators: Fred Roozeboom, Eindhoven University of Technology and TNO, Harm Knoops, Eindhoven University of Technology

2:30pm **ALE2-TuA5 Thermal Selective Etching on Metal Oxide and Nitride Film*, Jinhyung Park,*** Air Liquide Laboratories Korea, Republic of Korea

Highly selective etching of metal oxide, nitride and metal has been demonstrated by using metal fluoride. In addition, this etching was taking thermal dry etching without plasma assisted. Reports of thermal dry etching by using metal fluoride are very limited.1 In this work we conducted etching test between 150 and 450oC on various metal oxides, nitrides and metal substrate. Some results showed selective etching that only desired film was etched and non-desired film was not etched under same conditions. Etching rate and selective tendency was also compared. Not only flat surface, it was confirmed that metal fluoride worked for dry etching of a film in patterned wafer.

Figure 1

Figure 1. SEM image of thermal etching of ZrO2 deposited in patterned wafer

Figure 1 showed one example that etching of ZrO2 in trench by using NbF5 under different conditions. All etching results are analyzed by several methods such as ellipsometry, scanning electron microscopy (SEM), electron dispersive spectroscopy (EDS) and x-ray photoelectron spectroscopy (XPS). In this presentation, individual etching result of metal oxides (Nb2O5, Ta2O5, TiO2, ZrO2, HfO2, SiO2, Al2O3, Y2O3), metal nitrides (TiN, TaN, SiN), metal (W) and their comparison will be shown and discussed.

[1] P. C. Lemaire, G. N. Parsons, Chem. Mat. 29, 6653(2017).

2:45pm **ALE2-TuA6 Benefits of Atomic Layer Etching for Material Selectivity*, Thorsten Lill,*** *K.J. Kanarik, . Tan, I. Berry, . Vahedi, R. Gottscho,* Lam Research Corp.

For most critical etch applications such as pattern-transfer and 3D structure formation, an essential requirement is material selectivity. By material selectivity we refer to etching one material (X) preferentially to another material (Y), where the extent of selectivity is commonly denoted by the ratio X:Y for the relative amounts etched. Etching has had to be selective since the earliest years and the development of selective processes has been developed at least over the last 40 years of plasma etching. in this talk, we will discuss the strategies of selective etching and how atomic layer etching (ALE) helps. Both directional and isotropic ALE schemes will be discussed, as well as the basic underlying strategies in both. The insights will be vital for exploiting ALE in the fabrication of future devices.

3:00pm **ALE2-TuA7 Approaching Atomic Scale Precision for Etch Technology Needs in the Semiconductor Industry*, Robert Bruce,*** *J. Papalia, M. Sagianis, D. Montalvan, H. Miyazoe, N. Marchack, S. Engelmann,* IBM TJ Watson Research Center **INVITED**

As we advance beyond the 7nm technology node, the semiconductor industry has implemented ever more complex architecture for logic and memory devices. For example, stacked nanosheets are a potential successor to finFETs and the number of levels continue to rise in 3D-NAND memory. To enable manufacture of new 3D devices at this unprecedented level of scale and intricacy requires atomic precision in etching and patterning, both anisotropic and isotropic, with high selectivity of etching one material over a host of other materials. Atomic layer etching (ALE) is a concept with goal to achieve this atomic scale precision by separating the etch process into controlled, self-limited reactions.

Because a large part of integrated devices are composed of insulating materials such as SiOx and SiNx, it is essential to understand their fundamental etching behavior at the atomic scale. In this talk, the interaction of SiOx and SiNx in hydrofluorocarbon-based plasmas was investigated. Due to their differences in surface modification behavior, the etching process could be tuned so that SiOx etches selectively to SiNx, and vice versa. The etch process parameters that influence material selectivity were evaluated, and it was found that hydrogen content, ion energy and substrate temperature had significant impact to the etching behavior of SiNx. The possibility of improving selectivity by separating deposition and etching in a quasi-ALE approach is also studied. These important observations provide essential guidance to a wide range of dielectric etch applications, such as self-aligned contact etching and spacer etching.