Oxford Instruments Plasma Technology

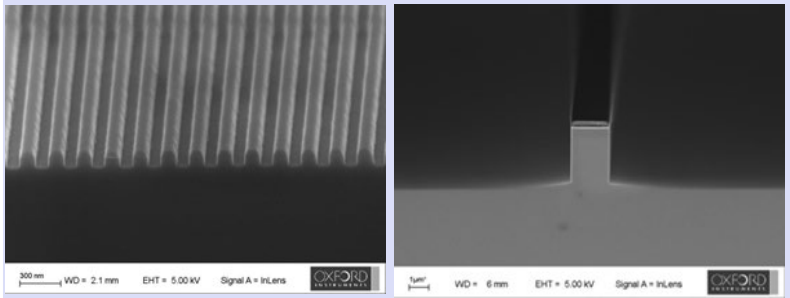
Customer Technical Update

December 2024

InP Lasers
Enabling More Good Wafers Today at a Lower Cost

Device Enabling Processes

Control of features allowing flexibility in device design **enabling efficient low optical loss, low damage devices** ideally suited for AI data centre applications



InP feature etch for EML and DFB lasers

- Minimal trenching
- Vertical profiles
- Smooth sidewall (low optical loss)
- Low damage (Hydrogen free)

Cost of Ownership

High throughput and low cost of ownership

Process Yield

- Hot electrostatic chuck (option 210 ˚C/250˚C) for fully automated single wafer processing
- Excellent process repeatability and tool to tool transfer

Wafer scaling

- 50mm – 100 mm as POR
- 150 mm InP first in fab

Throughput

- >4000 wpm 5 µm InP etch
- >1 µm/min InP etch
- 2500 µm between cleans with polymer free chemistry

The OI Difference

- **Market leader** in InP based processing
- **Largest install base** including market leading companies
- **First in Fab** fully automated 6" single wafer processing
- Extensive process **expertise** applied to solve challenges and enable next generation devices

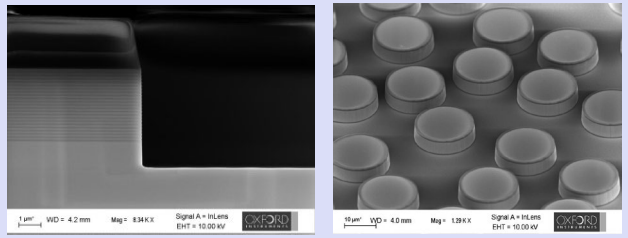
GaAs VCSELs
Enabling More Good Wafers Today at a Lower Cost

Device Enabling Processes

Flexible feature architecture and **high-quality atomic layer deposition (ALD) moisture barriers** ensuring every device is produced as designed for low optical loss, high yield and reliability

GaAs/AlGaAs mesa etch
- Minimal footing and zero trenching
- Vertical or sloped profiles
- Residue free sidewalls

ALD moisture barrier
- High quality SiN_x and Al_2O_3 ALD layers with very low moisture penetration



Cost of Ownership

High throughput and low cost of ownership

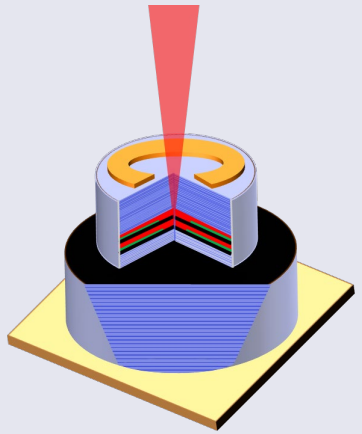
Process Yield
- Fully automated single wafer processing
- Excellent process repeatability and tool to tool transfer
- Interleave cleans during mesa etch to reduce cleaning overheads

Wafer scaling
- 100 mm and 150 mm as standard

Mesa Etch Throughput
- >2000 wpm 4.5 µm mesa etch
- >600 nm/min GaAs etch
- 7450 µm between cleans

The OI Difference

- **Production qualified** processing at market leading companies
- Low footing **mesa etch process** to enable complex geometries
- Unique **etch and ALD process** capabilities to enable next generation devices



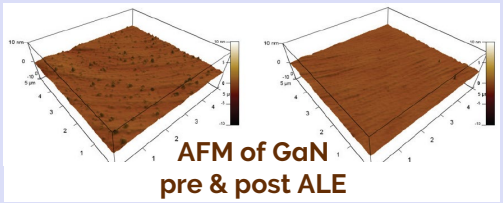
GaN Power Electronics & RF
Enabling More Good Wafers Today at a Lower Cost

Device Enabling Processes

Control of interfaces for improved device performance

Atomic Layer Etch (ALE): AlGaN, GaN

- Surface smoothing post etch
- Low damage controlled remote plasma etch



AFM of GaN pre & post ALE

Atomic Layer Deposition (ALD): SiO_x, AlO_x, HfO_x, AlN, SiN_x

- Native oxide removal by plasma pre-treatment
- Engineered material properties such as tuneable crystallinity nitrides
- Low damage plasma processing from innovative patented plasma source

Cost of Ownership

High throughput and low cost of ownership

Process Yield

- Patented endpoint for precise ≤1 nm etch depth control

Wafer scaling

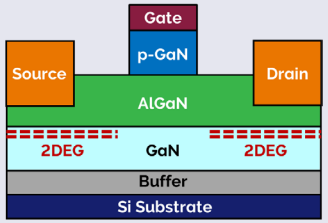
- 150 mm and 200 mm with rapid reconfiguration

Throughput

- ALD Al_2O_3 passivation >5000 wpm – CoO reduced by 75% compared to benchmark remote plasma
- ALE AlGaN etch > 2500 wpm

The OI Difference

- **ALD and ALE** for WBG materials qualified and ramping in p-GaN. cascode and MISHEMT devices
- Atomfab **ALD process of record** in HVM GaN HEMT manufacturing
- **Range of HVM** deposition and etch solutions for multiple device design and integration schemes
- **Qualified partner** solving key technology challenges at the atomic-scale for next generation GaN device manufacturing



SiC Power Electronics

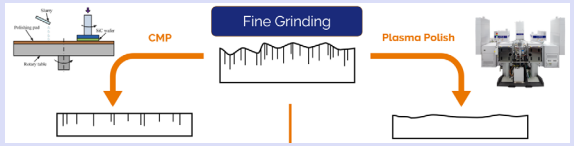
New processes to greener, better SiC devices at lower cost

Device Enabling Processes

Contactless polishing solution to prepare epi-ready substates

Plasma Polish Dry Etch

Cost effective, clean and green HVM substrate polishing solution designed to remove sub-surface damage.



Interface engineering to improve device characteristics

Bias Pulsed ALE: Improved interfaces

- Fast atomic layer etching to prepare defect-free interfaces.

ALD: Conformal dielectrics

- Defect-free conformal dielectrics for higher performing MOS interfaces.

Cost of Ownership

High throughput and low cost of ownership

Process Yield

- More reliable and improved process control

Wafer scaling

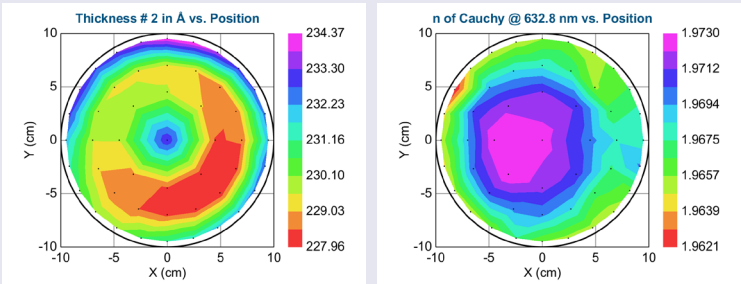
- 150 mm and 200 mm with rapid reconfiguration

Clustering of Technologies

- Ability to combine multiple material processing technologies in a single-cluster tool.

The OI Difference

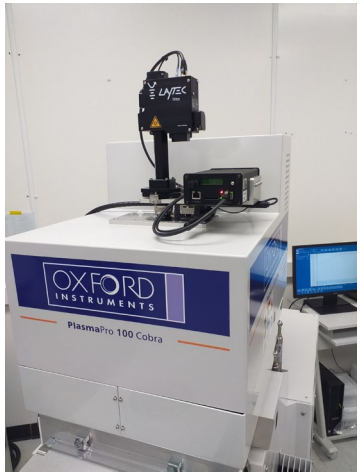
- **Plasma Polish** process qualified on MOSFET devices
- **ALD and ALE** process ready for customer demo
- **Qualified partner** solving key technology challenges on the atomic-scale for next generation in SiC device fabrication

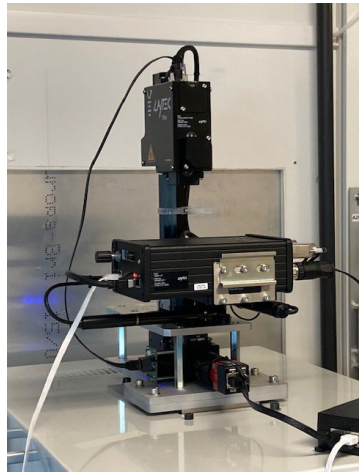


Example data for AlN ALD on 200 mm wafer size

Device enabling metrology

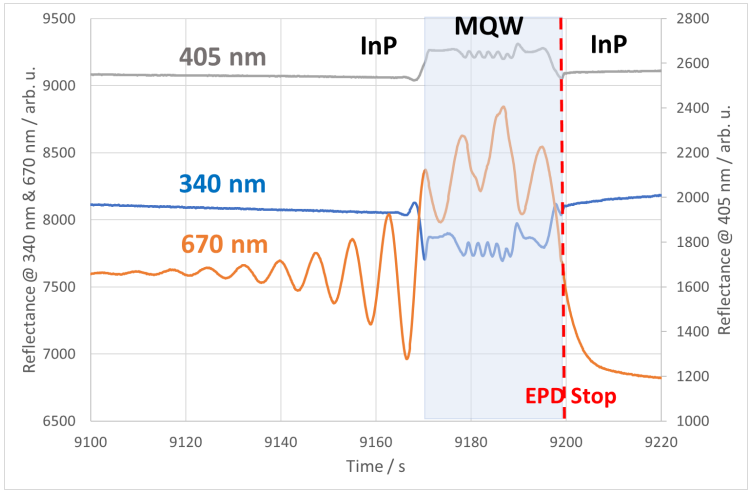
- In-situ metrology for plasma etch monitoring enabling reproducible and accurate endpoint detection
- Customizable system based on three wavelength operations suitable for different material systems, e.g. GaN, GaAs, InP
- Measurement of residual thickness and etch depth, detection of interface with nm-accuracy
- Automated endpoint algorithms
- High resolution camera module





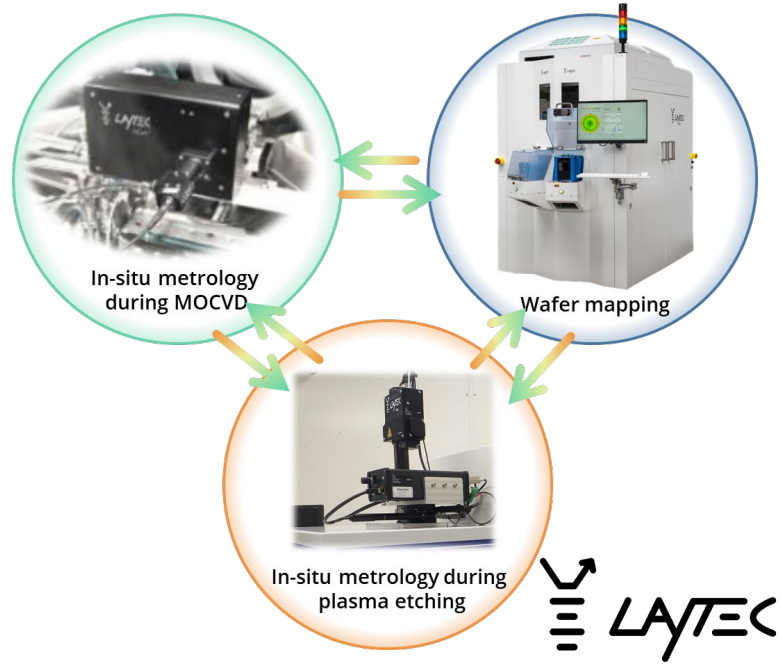
Cost of Ownership

- Fully automated and integrated endpoint detection for dry etch process control and high yield
- Excellent measurement precision and reproducibility for compensation of etch rate drift
- Endpoint for accurate etch depth control down to ≤ 1 nm
- Interface detection enabling switch from slow to fast etch processes, reducing manufacturing costs



The LayTec difference

- Market leader in in-situ and in-line optical metrology for wide range of thin film processes
- Expertise in optics, thin film application and physical modeling
- Cutting edge analysis features
- Connected metrology



LAYTEC
MEMBER OF THE NYNOMIC GROUP